REMARKS

Claims 1-20 are pending in the application. Claims 1-20 stand rejected. Applicant respectfully requests consideration of the following remarks and allowance of the claims.

Rejections Based Upon 35 U.S.C. § 103(a)

Claims 1-20 stand rejected as being unpatentable over Aybay (U.S. Patent No. 6, 185,221) in view of Olnowich (U.S. Patent No. 5, 920,704). Applicant respectfully disagrees and submits that the claims are allowable over the art of record for at least the following reasons.

Independent claim 1 requires crossbar integrated circuits configured to receive communications and a clock signal over *parallel* channels rather than serial channels. Specifically, claim 1 requires three elements: 1) parallel channels, 2) processing circuitry, and 3) crossbar integrated circuits. The processing circuitry is configured to exchange communications between communication links and the parallel channels. The crossbar integrated circuits are configured to receive the communications and a clock signal over the parallel channels.

In contrast, FIG. 5 of Aybay discloses a crossbar integrated switch as contemplated in the background section of applicant's Specification describing FIG. 2. In the prior art, crossbar integrated switches required serial channel interfaces to the crossbar switching matrix. FIG. 2 of applicant's Specification illustrates a crossbar integrated switch 202 in the prior art having serial channel interfaces 221-226 to a crossbar matrix 240.

Specifically, FIG. 5 of Aybaby discloses a preferred architecture of a multipoint switch. The switch in FIG. 5 includes a crossbar 60 and four (4) input modules to the crossbar 60. One of the input modules includes, for example, link 22, I/O control 12, and packet processing unit 82. Taken together, the elements of the input module provide a serial interface to crossbar 60. However, claim 1 requires crossbar integrated circuits that receive communications over *parallel* channels, not serial channels. For example, FIG. 4 of applicant's Specification illustrates crossbar integrated circuit 402 having *parallel* channel interfaces 421-426 to a crossbar matrix 440.

The Office Action characterizes Aybay as disclosing parallel channels at col. 2, lines 1-5. However, this section of Aybay describing FIG. 1 discloses parallel input *queues*, not parallel *channels*. In fact, the four input *channels* 12, 14, 16, and 18 are *serial* input channels (*Aybay*, col. 1, lines 35-45).

The Office Action cites Olnowich as disclosing a parallel clock. However, Olnowich does not disclose *processing circuitry* configured to exchange communications between serial communication links and parallel channels as required by independent claim 1. Rather, Olnowich only discloses an Allnode switch having several input nodes. The configuration or operation of the nodes is not disclosed or discussed. Furthermore, the Examiner has not provided any citations or reasoning to support the assertion that the input nodes of Olnowich are configured to exchange communications *between serial communication links and parallel channels* as required by claim 1.

Aybay and Olnowich, separately and in combination, do not teach or suggest all the elements of claim 1. Independent claim 11 contains limitations similar to those of claim 1 and is therefore allowable over the art of record for the same reasons as claim 1. The dependent claims contain otherwise allowable subject matter, but are also allowable in view of their dependence from allowable independent claims. Applicant forgoes a discussion of the dependent claims for the sake of brevity.

CONCLUSION

The claims in their present form are allowable over the art of record. Applicant therefore solicits their allowance.

SIGNATURE OF PRACTITIONER

Stephen S. Roche, Reg. No.
Duft Setter Ollila & Bornsen LLC
Telephone: (303) 938-9999 ext. 15
Facsimile: (303) 938-9995

Correspondence address: **CUSTOMER NO. 036122**